

**Clean version of all pending claims**

1-7. (Cancelled)

*Sub Bl*

8. (Amended once) A method, comprising:

using a conversion table to translate a first address from a graphics controller to a second address to a memory; and

using the conversion table to translate a third address from a bus controller to a fourth address to the memory;

wherein the second address has a greater number of bits than the first address and the fourth address has a greater number of bits than the third address .

9. (Amended once) The method of claim 8, wherein said using the conversion table to translate the third address includes using a translation lookaside buffer.

10-11. (Cancelled)

12. (Amended once) The method of claim 8, wherein said using the conversion table to translate the third address includes:

comparing a first portion of the third address with entries in a first table;

if the first portion matches a particular one of the entries in the first table,

combining a value associated with the particular one with a second portion of the third address to form the fourth address.

81  
Contd

13. (Amended once) The method of claim 12, further comprising:  
if the first portion does not match any of the entries in the first table, referring to  
a second table to translate the third address.

81  
Contd

14. (Amended once) The method of claim 13, wherein:  
said comparing includes comparing the first portion of the third address with  
entries in the first table in an input-output controller; and  
said referring to the second table includes referring to the second table in main  
memory.

15. (Amended once) An apparatus, comprising:  
a translation lookaside buffer coupled to an input register and an output register;  
control logic coupled to the translation lookaside buffer, the input register, and the  
output register;  
wherein the control logic is to compare a first portion of an initial address in the  
input register with entries in the translation lookaside buffer; and if a  
matching entry is found, to combine a first value associated with the  
matching entry with a second portion of the initial address to form a first  
translated address and hold the first translated address in the output  
register;  
wherein the first value has a greater number of bits than the first portion .

*31  
cont'd.*

16. The apparatus of claim 15, wherein the control logic is further to:  
access a table in memory if the matching entry is not found;  
find a second value in the table associated with the first portion;  
combine the second value with the second portion to form a second translated  
address; and  
hold the second translated address in the output register.

17. (Amended once) The apparatus of claim 16, wherein:  
the control logic includes logic for first and second control flows;  
the second control flow is to translate an initial graphics controller address and  
does not access the second table; and  
the first control flow is to translate an initial bus controller address and access the  
second table.

18. The apparatus of claim 16, wherein the first and second translated addresses each  
have more bits than the initial address.

19. (Amended once) A system, including:  
a processor;  
a memory;  
a graphics controller;  
a bus controller;

B1  
Cont'd.

an input-output controller coupled to the processor, memory, graphics controller and bus controller, the input-output controller including:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register;

wherein the control logic is to compare a first portion of a first initial address from the bus controller in the input register with entries in the translation lookaside buffer; and if a first matching entry is found, to combine a first value associated with the first matching entry with a second portion of the first initial address to form a first translated address and hold the first translated address in the output register;

wherein the control logic is further to compare a first portion of a second initial address from the graphics controller in the input register with the entries in the translation lookaside buffer; and if a second matching entry is found, to combine a second value associated with the second matching entry with a second portion of the second initial address to form a second translated address and hold the second translated address in the output register.

20. (Amended once) The system of claim 19, wherein the control logic is further to: access a table in memory if the first matching entry is not found;

*B1*  
find a third value in the table associated with the first portion of the first initial address;

combine the third value with the second portion of the first initial address to form a third translated address; and

hold the third translated address in the output register.

*ACV*

21. (Amended once) The system of claim 20, wherein:  
the control logic includes logic for first and second control flows;  
the second control flow is to translate an initial graphics controller address and does not access the table; and  
the first control flow is to translate an initial bus controller address and access the table.

22. (Amended once) The system of claim 20, wherein the first translated address has more bits than the first initial address and the second translated address has more bits than the second initial address .

*B*

23. (Amended once) A machine-readable medium having stored thereon instructions, which when executed by a machine cause said processor to perform:  
reading a first address containing a first number of bits and having an upper portion and a lower portion;  
comparing the upper portion with a plurality of first entries in a first table;  
if the upper portion matches a particular one of the plurality of first entries:

selecting a second entry in the first table associated with the particular one of the plurality of first entries;

combining the second entry with the lower portion to form a first translated address; and

transmitting the first translated address;

wherein the second entry contains a greater number of bits than the upper portion.

24. The medium of claim 23, further comprising:

if the upper portion does not match any of the plurality of first entries in the first table:

accessing a second table having a plurality of third entries;

indexing the second table with the upper portion to identify a particular one of the plurality of third entries;

combining the particular one of the plurality of third entries with the lower portion to form a second translated address; and

transmitting the second translated address.

25. The medium of claim 24, wherein the first table is contained in an input-output controller and the second table is contained in main memory.

26. (Amended once) The medium of claim 24, wherein said transmitting the first translated address includes transmitting to a memory controller.

27. The medium of claim 23, wherein the first table is a translation lookaside buffer.

28. (Amended once) The medium of claim 23, wherein said reading a first address includes reading a first address from a bus controller.

29. The medium of claim 28, wherein the first table is also used to translate addresses from a graphics controller.

*A2 B1*  
30. (New) An apparatus comprising:

an address translator having a first interface to couple to a memory controller, a second interface to couple to a graphics controller, a third interface to couple to a bus controller, and a table of entries, each entry having a first portion and a second portion; a translation control circuit coupled to the address translator to program the entries in the address translator;

wherein the address translator is to translate an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface.

31. (New) The apparatus of claim 30, wherein:

the address translator is further to translate an address on the second interface into a second address on the first interface having a greater number of bits than the address on the second interface.